Paper No. 40

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte VISHRAM P. DALVI
and RODNEY R. ROZMAN

Appeal No. 2002-1578
Application No. 08/814,928

ON BRIEF

Before BARRETT, RUGGIERO, and DIXON, Administrative Patent Judges.
RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 31-37, which are all of the claims pending in the present application. Claims 1-11, 20-25, and 30 have been canceled. Claims 12-19 and 26-29 stand withdrawn from consideration as being directed to a non-elected invention.

The claimed invention relates to a memory device which includes a status register for indicating the suspend status of a programming operation. On indication of the suspension of a

programming operation to a specific location, the system processor has an opportunity to request that a data modification operation to another memory location be performed while the programming operation is suspended.

Representative claim 31 is reproduced as follows:

31. A memory device, comprising:

a memory array;

a register to store at least one bit indicating a suspend status of a write operation for the memory array; and

a control circuit coupled to said memory array and said register, said control circuit to update said register and to control an output of a status signal representing said suspend status of said write operation, and wherein said control circuit includes:

a first state machine to receive commands for accessing said memory array or said register, and

a second state machine coupled to said first state machine and to execute the commands received by said first state machine.

The Examiner relies on the following prior art references:[1]

Terada et al. (Terada)	5,561,628	Oct. 01, 1996
Leak et al. (Leak)	5,937,424	Aug. 10, 1999 (filed Feb. 27, 1997)

Claims 31-37, all of the appealed claims, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Appellants' admitted

[1] In addition, the Examiner relies on Appellants' admissions as to the prior art at pages 1-3 of Appellants' specification.

prior art. In separate rejections under 35 U.S.C. § 103(a), claims 31-37 stand rejected as being unpatentable over Terada alone and as being unpatentable over Leak in view of Terada.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs[2] and Answer for the respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the Examiner, the arguments in support of the rejections, and the evidence of obviousness relied upon by the Examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the

[2] The Appeal Brief was filed October 17, 2001 (Paper no. 34). In response to the Examiner's Answer dated February 8, 2002 (Paper No. 35), a Reply Brief was filed March 5, 2002 (Paper No. 36), which was acknowledged and entered by the Examiner as indicated in the communication dated March 29, 2002 (Paper No. 37).

art the obviousness of the invention as set forth in claims 31-37. Accordingly, we affirm.

Appellants indicate (Brief, page 6) that the claims on appeal stand or fall together as a group. Consistent with this indication, Appellants' arguments are directed solely to features which are set forth in independent claim 31. Accordingly, we will select independent claim 31 as the representative claim for all the claims on appeal, and claims 32-27 will stand or fall with claim 31. Note In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

As a general proposition in an appeal involving a rejection under 35 U.S.C. § 103, an Examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

With respect to representative independent claim 31, the Examiner (Answer, pages 7-9) proposes to modify the semiconductor memory device disclosure of Leak. According to the Examiner (id., at 8), Leak, which discloses the advantages of suspending both erase and write operations while performing a read operation to increase system performance, discloses the claimed invention except for an explicit description of a status register with a bit indicator to represent a suspend state. To address this deficiency, the Examiner turns to Terada which describes a status register with a bit indicator such as an "ESS" bit to indicate that an erase operation has been suspended. In the Examiner's analysis (id., at 8 and 9), the skilled artisan would have recognized and appreciated the obviousness of modeling the status register of Leak after that of Terada to provide a bit indication of suspend status especially in view of the fact that Leak provides a clear teaching of outputting status data in response to a read operation.

After reviewing the Examiner's analysis (Answer, pages 4-6), it is our view that such analysis carefully points out the teachings of the Leak and Terada references, reasonably indicates the perceived differences between this prior art and the claimed invention, and provides reasons as to how and why the prior art teachings would have been modified and/or combined to arrive at the

claimed invention. In our opinion, the Examiner's analysis is sufficiently reasonable that we find that the Examiner has at least satisfied the burden of presenting a prima facie case of obviousness. The burden is, therefore, upon Appellants to come forward with evidence and/or arguments which persuasively rebut the Examiner's prima facie case of obviousness. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Brief have not been considered [see 37 CFR § 1.192(a)].

Appellants' arguments in response to the obviousness rejection based on the combination of Leak and Terada assert that the Examiner has failed to establish a prima facie case of obviousness since all of the claimed limitations are not taught or suggested by the applied prior art references. After careful review of the applied Leak and Terada references in light of the arguments of record, we find Appellants' assertions to be unpersuasive. In our view, Appellants' arguments unpersuasively focus on the individual differences between the limitations of representative claim 31 and each of the applied references. It is apparent, however, from the Examiner's line of reasoning in the Answer, that the basis for the obviousness rejection is the combination of Leak and Terada. One cannot show nonobviousness by attacking references individually

where the rejections are based on combinations of references. In re Keller, 642 F. 2d 413, 425, 208 USPQ 871, 881(CCPA 1981); In re Merck & Co., Inc., 800 F. 2d 1091, 1096, 231 USPQ 375, 380 (Fed. Cir. 1986).

In other words, while Appellants contend (Brief, page 16) that Leak lacks a teaching of providing a status register with a bit indication representative of an operation suspend status, such a bit indication status register is clearly taught by Terada. Similarly, although Appellants argue (id.) that Terada fails to teach the suspension of a write operation, this teaching is specifically provided by Leak.

We further find to be unpersuasive Appellants argument (Brief, page 16) in support of the contention that the Examiner has failed to provide proper motivation for the proposed combination of Leak and Terada so as to establish a prima facie case of obviousness. In our view, Appellants' arguments notwithstanding, the fact that the Terada reference is concerned with testing of flash memory devices does not mitigate its clear teaching of providing a status register with a bit indicator to represent the status of an operation.

For the above reasons, since it is our opinion that the Examiner's prima facie case of obviousness based on the combination of Leak and Terada has not been overcome by any convincing arguments from Appellants, the Examiner's 35 U.S.C. § 103(a) rejection of representative independent claim 31, as well as claims 32-37 which fall with claim 31, is sustained.

Turning to a consideration of the Examiner's separate 35 U.S.C. § 103(a) rejections of appealed claims 31-37 based on each of, in the alternative, Appellants' admitted prior art and Terada, we cannot sustain either of these rejections. The Examiner's basis for each of these rejections relies on statements in the admitted prior art (Appellants' specification, page 1) and Terada (column 5, lines 5-11) directed to the differences in time for performing erase, write, and read operations. As correctly recognized by the Examiner, both the admitted prior art and Terada explicitly recognize the advantages of suspending an erase operation in order to perform write and read operations because of the longer time required to perform an erase operation relative to write and read operations. From these prior art teachings, however, the Examiner draws the unsupported conclusion as to the obviousness to the skilled artisan of suspending a write operation in order to perform

a read operation because of the longer time required to perform a write operation relative to a read operation.

As noted above, the Examiner has the burden of initially presenting a prima facie case of obviousness. The Examiner cannot satisfy this burden by simply dismissing differences between the claimed invention and the teachings of the prior art as being obvious. The Examiner must present us with an evidentiary record which supports the finding of obviousness. It does not matter how strong the Examiner's convictions are that the claimed invention would have been obvious, or whether we might have an intuitive belief that the claimed invention would have been obvious within the meaning of 35 U.S.C. § 103. Neither circumstance is a substitute for evidence lacking in the record before us. While further study and scrutiny of the Examiner's analysis might eventually convince us of the correctness of the Examiner's position, we do not find this to be necessary. It is quite clear to us that the very issue which the Examiner has gone to great pains to establish the obviousness to the skilled artisan, i.e., the advantages of suspending a write operation to perform a read operation because of the longer performance times of a write operation relative to a read operation, is explicitly recognized and taught by the Leak reference as discussed supra.

In summary, with respect to the Examiner's 35 U.S.C. § 103(a) rejections of appealed claims 31-37, we have not sustained the alternative rejections based on the admitted prior and Terada, but have sustained the rejection based on the combination of Leak and Terada. Therefore, the decision of the Examiner rejecting claims 31-37 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

LEE E. BARRETT
Administrative Patent Judge

JOSEPH F. RUGGIERO
Administrative Patent Judge

JOSEPH L. DIXON
Administrative Patent Judge

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